# Optical coupling to monolithic integrated photonic circuits

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## ABSTRACT

Methods of coupling optical fiber and light sources to monolithic integrated photonic circuits are needed to expand future photonics communications markets. Requirements are low cost, high coupling efficiencies, and scalability to high volume production rates. Key features of the different optical coupling options will be discussed along with implementation examples. Requirements for low cost optical coupling and high volume production scalability will be shared.

**Keywords:** optical coupling, monolithic, photonic integrated circuit (PIC), low cost

## 1. INTRODUCTION

Optical coupling to monolithic structures has remained a technical and cost challenge for wider spread implementation of integrated photonic circuits. Monolithic integration of photonic components in either silicon or III-V material offers the possibility of dramatically reduced costs for optical communication functionality based upon wafer scale batch fabrication advantages. This has been demonstrated in recent years by photonic integrated circuit (PIC) products by Luxtera in Si [1] and by Infinera in InP [2].

Low cost optical coupling methods have remained illusive for photonic communication devices as well as for recent PICs. This is due to both the technical challenges in optical coupling to single mode waveguides and also due to the relatively small market size for photonic communications applications.

Technical challenges for coupling optical power of signals from optical fiber to planar waveguides include:

1. High coupling efficiency requirement
2. Tight (micrometer & submicrometer) alignment tolerances
3. Waveguide size and shape differences between planar waveguides and optical fiber
4. High refractive index contrast with Si and III-V materials
5. Optical wavelength choice, (e.g. silicon is opaque at wavelengths below 1100nm)
6. Large number of optical components, submounts and subassemblies
7. Large number of align and attachment assembly steps
8. Large optical component size relative to monolithic photonic circuits
9. Issues in handling fiber pigtail volume
10. Incompatibility of traditional photonic designs with electronic industry standard automated assembly processes
11. Incompatibilities of traditional planar lightwave circuits (PLC) with electronic integrated circuit (IC) fabrication processing
12. Need for optoelectronic testing of circuits in the manufacturing process and to determine known-good-die (KGD) at the wafer level

Figure 1 shows the correlation between current photonics communication device markets and future market applications with cost per device and market size in terms of number of units. There is a cost barrier for existing optical coupling technologies at $10 per transponder. High volume markets of chip-to-chip optical communication require new coupling technologies to reach this application's lower cost points.

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Figure 2 roadmaps progressive integration paths from traditional high cost individually packaged photonic components (top left) to a potentially ultimate monolithic integration of photonics with electronics (bottom right) where all signals on and off the chip are optical and only power and ground are electrical interconnects. Transition paths from electrical to optical interconnects have been predicted to be as early as 2008 for board-to-board communication and as early as 2010 for chip-to-chip communication[3]. PIC products fabricated in Si by complementary metal-oxide semiconductor (CMOS) compatible processing have been fielded for server transponders[1] and fabricated in InP for telecommunications Dense-Wavelength-Division-Multiplexed (DWDM) transponder applications[2]. Optical motherboards using silicon optical bench (SOB) micromachining have seen integration in low cost transponders, but have yet to see integration on computing platforms. An alternative approach of integrating optical coupling in printed circuit boards (PCB) with backplane optical interconnects has not been commercialized. In all integration paths, low cost optical coupling methods are necessary. This paper shall focus on optical coupling to monolithic PICs and a sister paper[4] details low cost optical interconnect developments.

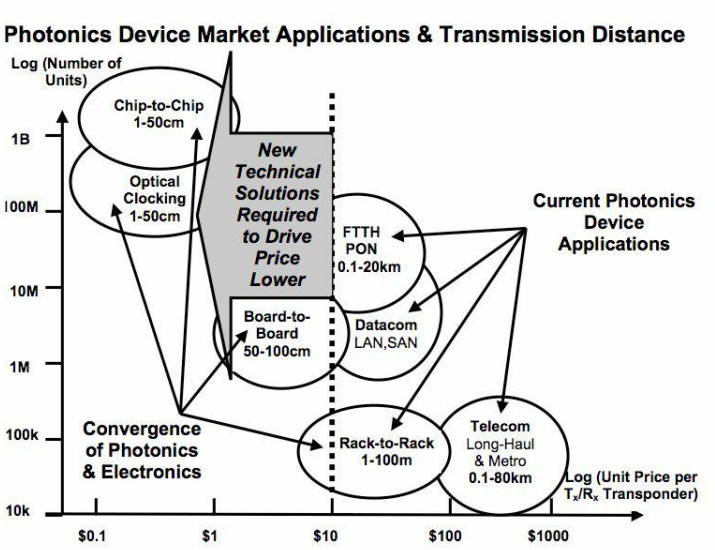


Fig. 1. Market size and device cost for photonics communications markets.

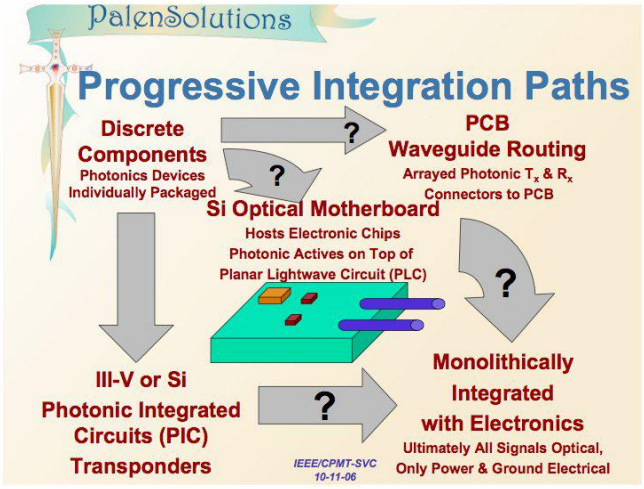


Fig. 2. Integration pathways from discretely packaged photonic components to photonic circuits monolithically integrated with electronics[5].

## 2. COUPLING OPTIONS

There are three options for coupling to a monolithic photonic integrated circuit:

1. At the edge
2. On the front-side
3. On the back-side

### 2.1 Edge coupling

Optical coupling at the edge of a monolithic PIC is similar to coupling to edge emitting lasers or edge coupling of waveguide arrays. Coupling to edge emitting lasers has remained an expensive packaging configuration. Coupling options may entail use of a single free space lens, two lenses, or a lens formed at the fiber tip with either conical or wedge lens shapes. In all cases submicrometer optical alignment tolerances are required in at least two axes (x and y). High coupling costs are due to these tight align and attachment tolerances which require: specialized align & attachment processing; submount structures for the laser chips and free space optical coupling elements; and hermetic packaging and feedthroughs. Costs for processing the laser chip are also substantial due to optical coating of the laser edge facet, usually performed at laser bar level, and burn-in testing at the laser bar level. Free space edge coupling to PIC waveguides requires anti-reflection (AR) coatings on the edge of the monolithic chip, which is a costly process requiring substantial handling of the chip. Coupling configurations using tapered or inverse tapered waveguides have additional alignment tolerance requirements.

Edge coupling of arrays of optical fibers to arrays of waveguides in arrayed waveguide gratings (AWG) PLCs has been by butt coupling of an angle polished edge of the PLC to a polished subassembly of fibers aligned in a silicon optical bench v-groove array. The v-grooves are set at the waveguide pitch and alignment requires 6 axis (x, y, z, theta, pitch and roll) active feedback motion control. Adhesive attachment with refractive index matching material is used. Coupling costs are high due to edge surface preparations, custom assembly equipment and slow processing times. Coupling efficiencies may also limited due mismatch of waveguide geometries from rectangular PLC waveguides to circular or oval optical fiber cores. Butt coupling to PIC waveguides requires an expansion of the PIC waveguide to match the fiber core size.

All edge coupling options do not allow for wafer level optoelectronic testing.

Edge coupling has been used for InP PICs in DWDM markets[2]. However, edge coupling options are not low cost solutions.

### 2.2 Front-side coupling

Front-side coupling may be made by:

1. Optical fiber in SOB v-grooves butt coupled to etched facets of planar waveguides
2. Evanescent coupling
3. Diffraction grating coupling, or
4. Projection coupling with lenses and turning mirrors

Coupling may be made via butt coupling an optical fiber in a SOB v-groove to an etched facet in the monolithic waveguide as shown in Figures 2 and 3. The waveguide is adiabatically expanded to match the larger mode field size of the fiber. Precision v-grooves are etched into <100> silicon wafers using anisotropic KOH etch and aligned to the waveguides by photolithography. Coupling is made by pressing a cleaved optical fiber stripped of its buffer into the v-groove and securing the fiber with index matching adhesive. This method of coupling has been implemented in Transmitter Optical Sub-Assemblies (TOSA) modules[6] and in Fiber-To-The-Home (FTTH) Passive-Optical-Network (PON) biplexer and triplexer modules[6].

Photonic circuit waveguides need to be close to the chip surface for evanescent mode coupling between parallel waveguides and for adiabatic coupling between parallel inverse tapered waveguides. Evanescent coupling configurations are difficult due to submicrometer vertical separation tolerances of the waveguides. Adiabatic coupling has been implemented for coupling lasers through a "Laser Surface Mount Converter" [6,7] at ±2 !m alignment tolerance to PLC waveguides. This coupling attachment effectively seals the optical path, thus removing the need for hermetic sealing for laser reliability. Evanescent coupling of planar waveguides with optical fiber is extremely difficult due to submicrometer tolerance control in removing fiber cladding and in maintaining evanescent contact distance with the planar waveguide.

Optical coupling to PIC waveguides may be made via diffraction gratings. Gratings are low cost as they are lithographically aligned and formed by wafer level etch processing. High refractive index contrast gratings and mirror metallization are required for high coupling efficiencies. Optimized coupling is made at small angles off normal from the chip as illustrated in Figure 4. Diffraction grating coupling efficiency is sensitive to light polarization and wavelength. Diffraction grating couplers have been implemented in silicon monolithic photonic circuits as "holographic lens" configurations at 1 !m alignment tolerance and with coupling efficiencies of up to -1.4dB (73%) into 0.1 $!m^2$ silicon-on-insulator (SOI) waveguides from optical fiber and from surface mounted lasers on the chip front-side[1]. This coupling method works with both ridge waveguides and buried waveguides.

Another coupling approach is to use lens systems to focus light to monolithic waveguides via 45° turning mirrors. Methods of fabricating the turning mirror include anisotropic KOH wet etch of off-angle cut <100> silicon wafers. AR coating is required as well as specialized mount structures to hold coupling optics. This coupling method is not PDL or wavelength sensitive.

Front-side coupling allows for wafer level optoelectronic testing. Coupling through PIC Back-End-Of-Line (BEOL) layers to buried waveguides requires metallization stay-out windows. Coupling through PIC Front-End-Of-Line (FEOL) dielectric layers to buried waveguides requires an understanding of their optical properties.

### 2.3 Back-side coupling

Optical coupling may be made to waveguides located on the chip front-side via the chip back-side. The two methods described above of diffraction gratings and focus into waveguides using turning mirrors may be used.

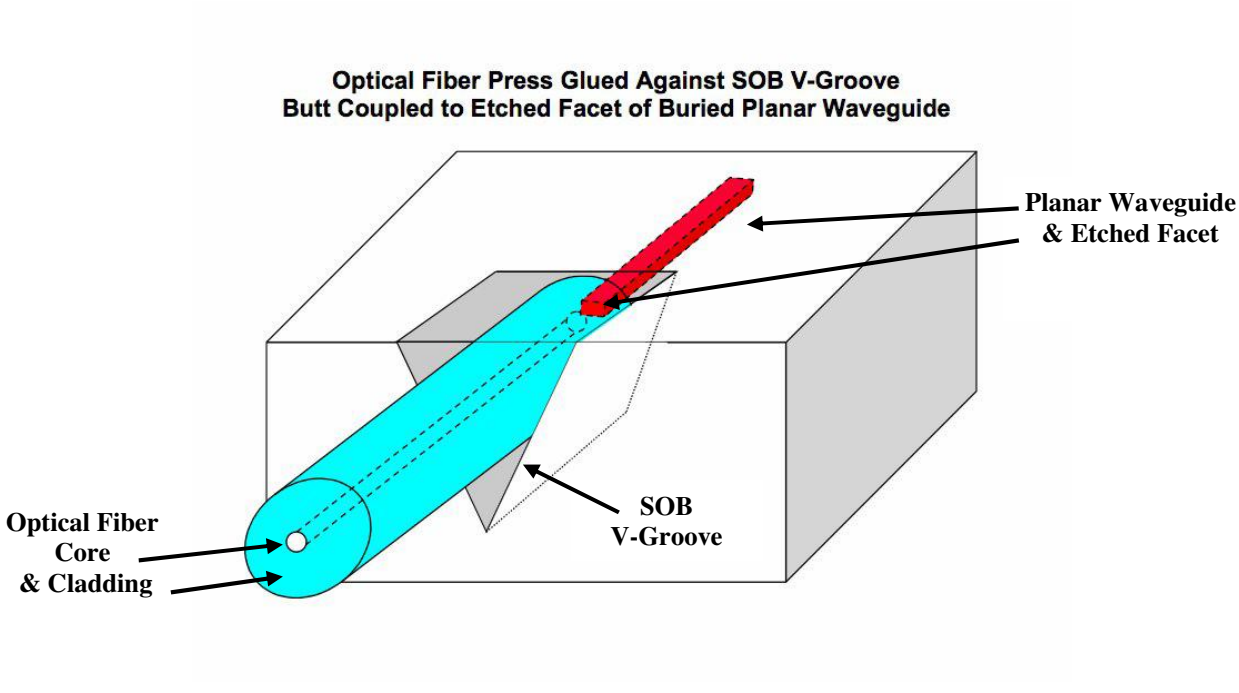


Fig. 3. Butt coupling of optical fiber in SOB v-groove to PLC waveguide.

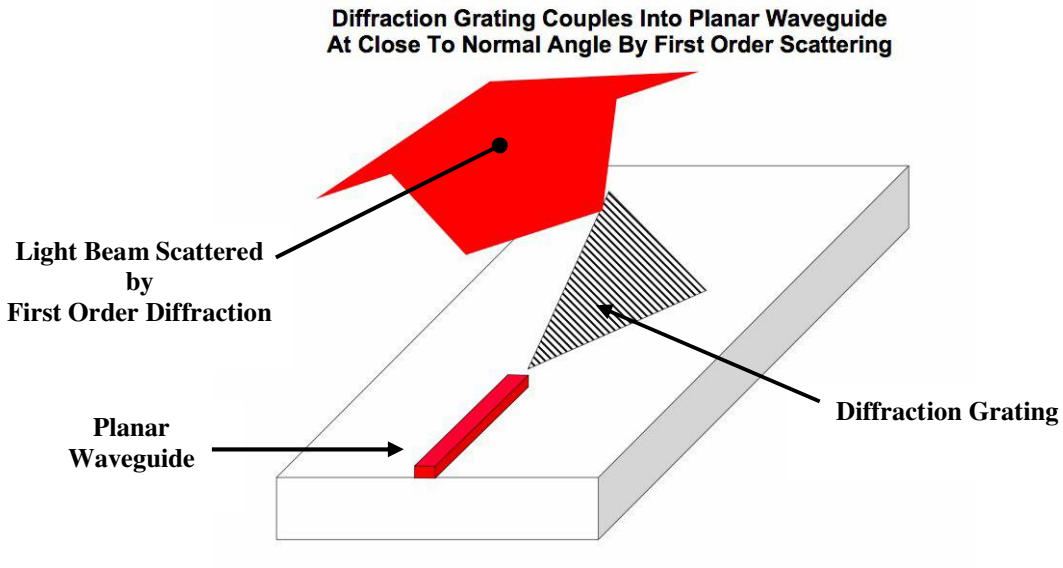


Fig. 4. Diffraction gating coupling to photonic chip.

## 3. FUTURE DIRECTIONS

Low cost coupler developments for optical coupling to PICs are likely to use projection coupling across the photonic chip front-side and back-side. Optical couplers for fibers, laser chips or photodetector chips to planar waveguides will include out-of-plane beam turning elements.

Low cost designs are likely to utilize fabrication techniques such as injection molding of plastic optical subassemblies for fiber couplers. Characteristics of these subassemblies are could include integrated lenses and passive fiber alignment pigtail attachment in very small form factors. Optical alignment tolerances will continue to increase to greater than 1 !m to enable lower cost assembly align and attach processing.

These low cost optical coupling solutions will be compatible with electronics industry standard surface mount assembly processing with passive optical alignment and fast attachment times.

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